What is claimed is:

1. A switched-mode Class F power amplifier configured for parallel connection with at least one other said amplifier for combining signals output from such parallel connected amplifiers, said amplifier comprising:

(a) an input component comprising at least one active device configured to be alternately switched by a signal input thereto to present an amplified signal corresponding to said input signal, said amplified signal constituting a low output impedance voltage source;

(b) an output resonator component; and,

(c) a lumped element impedance inverter between said input component and said output component, said impedance inverter configured for transforming said low output impedance voltage source so as to constitute a high output impedance current source, and said high output impedance current source configured for said parallel connection;

wherein negative reactive component values required by said impedance inverter are eliminated and effectively provided by incorporating said values into pre-selected reactive components of said input and output components.

2. A switched-mode power amplifier according to claim 1 wherein said input signal is an analog phase modulated signal.

3. A switched-mode power amplifier according to claim 1, wherein a source-drain parasitic capacitance across said active device is eliminated by one or more pre-selected reactive components of said input component, the value(s) of said pre-selected reactive components being pre-determined to

effectively compensate for said parasitic capacitance.

4. A method for amplifying an input signal to produce an output signal configured for parallel connection with at least one other like output signal for combining said output signals within a Chireix circuit architecture, said method comprising:

(a) amplifying said input signal by means of at least one active device configured to be alternately switched by said input signal and presenting an amplified signal corresponding to said input signal, said amplified signal constituting a low output impedance voltage source;

(b) providing across said active device a second harmonic resonator configured for shorting a second harmonic signal of said input signal;

(c) transforming said low output impedance voltage source to constitute a high output impedance current source by means of a lumped element impedance inverter, said high output impedance current source configured for said parallel connection; and,

(d) providing a third harmonic resonator configured for blocking a third harmonic signal of said input signal from a load connected to said output signal;

whereby negative reactive component values required by said impedance inverter are eliminated and effectively provided by incorporating said values into pre-selected adjacent reactive components of said resonators.

5. A method according to claim 4 whereby said input signal is an analog phase modulated signal.

6. A method according to claim 5 and further comprising eliminating a source-drain parasitic capacitance across said active device by one or more pre-selected reactive components of said second harmonic resonator the value(s) of which are selected to effectively compensate for said parasitic capacitance.

7. A plurality of switched-mode Class F power amplifiers in parallel connection for combining signals output from said amplifiers, said parallel-connected amplifiers comprising:

(a) an input component for each of said plurality of amplifiers, each said input component comprising at least one active device configured to be alternately switched by a signal input thereto to present an amplified signal corresponding to said input signal, said amplified signal constituting a low output impedance voltage source;

(b) a common output resonator component for said plurality of amplifiers; and,

(c) a lumped element impedance inverter for each of said plurality of amplifiers between said input component and said output component, said impedance inverter configured for transforming said low output impedance voltage source so as to constitute a high output impedance current source and said high output impedance current source configured for said parallel connection;

wherein negative reactive component values required by said impedance inverter are eliminated and effectively provided by incorporating said values into pre-selected reactive components of said input and output components.